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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/872,475	06/01/2001	Richard Shann	858063.452	9501

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EXAMINER	
TANG, KUO LIANG J	

ART UNIT	PAPER NUMBER
2122	

DATE MAILED: 11/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/872,475	SHANN ET AL.
	Examiner	Art Unit
	Kuo-Liang J Tang	2122

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *7/29/2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the amendment filed on 7/29/2004.

Claims 1-22 are pending and have been examined. The priority date for this application is 06/01/2000.

Response to Arguments

2. Applicant's arguments, see pages 7-10, filed 7/29/2004, with respect to Claims 1-22 have been fully considered and are persuasive. The rejection of Claims 1-22 has been withdrawn.

3. Claims 1-7 and 10-22 remain rejected under 35 U.S.C. 103(a) as being unpatentable over Chamberlain in view of Ohde.

Claims 8-9 remain rejected under 35 U.S.C. 103(a) as being unpatentable over Chamberlain in view of Charles.

In the remarks, the applicant argues that:

1. The Applicant argues that Chamberlain article as a date ("March 16, 1999") on which the document "was generated", there is no information to suggest that this was the actual publication date of the article.

2. As for independent claims 1 and 18, the Applicant argues that jump instructions referred to in Chamberlain are part of the actual object code that linker is combining, rather than

an instruction that controls how the linker reads the next relaxation instruction. (see RE page 9, lines 5-8).

Examiner's response:

1. The Chamberlain article was provided by the Applicant as IDS and the date shown is "March 16, 1999".

2. The examiner disagrees with Applicant's assertion that Chamberlain are part of the actual object code that linker is combining because it is not in the claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-7 and 10-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chamberlain et al., "Using ld The GNU linker ld version 2 version 2.9.4", pages 1-73, March 1999 (art of record, hereinafter Chamberlain) in view of Ohde et al., US Patent No. 5,511,207 (hereinafter Ohde).

As Per Claim 1, Chamberlain teaches that ld combines a number of object and archive files, relocates their data and ties up symbol references. Usually the last step in compiling a program is to run ld. ld accepts Linker Command Language files written in a superset of AT&T's Link Editor Command Language syntax, to provide explicit and total control over the

linking process. (E.g. see page 1 Overview and associated text). In that Chamberlain discloses the method that covering the steps of:

(a) reading (E.g. see page 1, line 8) each relaxation (E.g. see page 10, lines 33-41, option –relax and see page 49, lines 11-13, relaxing address mode) instruction in the ordered sequence defined by the sequence of instruction counts; and

(b) where said relaxation instruction is of the first type defining a relocation operation (E.g. see page 53, line 21), executing that relocation operation on section data to which it relates, and where said relaxation instruction is a jump relaxation instruction (E.g. see page 49, line 12, jsr and jmp), the next relaxation instruction which is read is that of the instruction count specified in the jump relaxation instruction (E.g. see page 49, line 13, bsr and bra).

Chamberlain does not explicitly disclose the sequence of instruction counts. However, Ohde in an analogous art teaches "the sequence of instruction counts". (E.g. see col. 8:1-37). Therefore, it would have been obvious to incorporate the teaching of Ohde into the teaching of Chamberlain to include the sequence of instruction counts. The modification would have been obvious because one of ordinary skill in the art would have been motivated so that the sequence of instructions being read out from memory and executed by the count order information.

As Per Claim 2, the rejection of claim 1 is incorporated and further Chamberlain teaches:

"recording a pass value indicative of the number of times said ordered sequence of relaxation instructions has been repeated." (E.g. see page 33, lines 28-29, the number of time is (&_bend - &_bstart)).

As Per Claim 3, the rejection of claim 2 is incorporated and further Chamberlain teaches:

"detecting when a result of a relocation operation executed on said section data has changed between repetitions of said ordered sequence of relaxation instructions and recording a change value indicative of the occurrence of said change." (E.g. see page 33, lines 28-29, dst).

As Per Claim 4, the rejection of claim 1 is incorporated and further Chamberlain teaches:

"said first type of relaxation instruction specifies an offset (E.g. see page 33, line 34, "ORIGIN = 0x1000" and associated text) and number of bytes (E.g. see page 33, line 34, "LENGTH = 0x1000" and associated text) of section data to be copied to said executable program (E.g. see page 33, line 35)".

As Per Claim 5, the rejection of claim 1 is incorporated and further Chamberlain teaches:

"said first type of relaxation instruction specifies a byte (E.g. see page 53, line 24-25) of section data to be copied to said executable program" .

As Per Claim 6, the rejection of claim 1 is incorporated and further Chamberlain teaches:

"said relaxation instruction of the second type includes a conditional relaxation instruction (E.g. see page 33, line 24, while loop) which specifies a number of subsequent relaxation instructions to be skipped in response to a condition being met (E.g. see page 33, lines 24-26, while loop")".

As Per Claim 7, the rejection of claim 1 is incorporated and further Chamberlain teaches:

"said relocation instruction to be executed specifies a number (E.g. see page 33, line 34, "LENGTH = 0x1000" and associated text) of subsequent relaxation instructions which are to be repeatedly subsequently read until a condition is met." (E.g. see page 53, line 24-25).

As Per Claim 10, Chamberlain teaches:

"a relaxation module for reading (E.g. see page 1, line 8) the relaxation instructions (E.g. see page 10, lines 33-41, option –relax and see page 49, lines 11-13, relaxing address mode) in an ordered sequence defined by the sequence of instruction counts, and executing said relaxation instruction;"

"a section data module for holding section data (E.g. see page 16 line 29 to page 17, line 2); wherein, when said relaxation instruction defines a relocation operation (E.g. see page 53, line 21), the relaxation module executes said relocation operation on section data defined in one or more previous relaxation instructions (E.g. see page 33, lines 8-16) and, when said relaxation instruction identifies section data, said section data is copied to said executable program, said section data being relocatable by subsequent previous relocation operations (E.g. see page 33, lines 8-16, e.g. ".text", ".mdata" and ".bss")" .

Chamberlain does not explicitly disclose the sequence of instruction counts. However, Ohde in an analogous art teaches "the sequence of instruction counts". (E.g. see col. 8:1-37). Therefore, it would have been obvious to incorporate the teaching of Ohde into the teaching of Chamberlain to include the sequence of instruction counts. The modification would have been obvious because one of ordinary skill in the art would have been motivated so that the sequence of instructions being read out from memory and executed by the count order information.

As Per Claims 11-12, the rejection of claim 10 are incorporated and are rejected under the same reason set forth in connection of the rejection of claims 2-3, respectively.

As Per Claims 13-17, the rejection of claim 10 are incorporated and are rejected under the same reason set forth in connection of the rejection of claims 4-5, 8-9 and 6 respectively.

As Per Claim 18, is the computer program product claim corresponding to the method claim 10 and is rejected under the same reason set forth in connection of the rejection of claim 10.

As Per Claim 19, Chamberlain teaches:

"(a) reading (E.g. see page 1, line 8) each relaxation instruction (E.g. see page 10, lines 33-41, option –relax and see page 49, lines 11-13, relaxing address mode) of the ordered sequence;" and

"(b) where said relaxation instruction is of the first type defining a relaxation operation (E.g. see page 53, line 21), executing that relocation operation on section data (E.g. see page 16 line 29 to page 17, line 2) to which it relates, and where said relaxation instruction is a jump relaxation instruction (E.g. see page 49, line 12, jsr and jmp), the next relaxation instruction which is read is that of an instruction count (E.g. see page 49, lines 12-13, which states "turns them into eight-bit program-counter relative bsr and bra instructions, respectively") specified in the jump relaxation instruction and where the relaxation instruction is a conditional relaxation

instruction (E.g. see page 33, lines 24-26, while loop), accessing a state variable which denotes linker state to determine whether the condition is satisfied."

As Per Claims 20-21, the rejection of claim 19 are incorporated and are rejected under the same reason set forth in connection of the rejection of claims 11-12, respectively.

As Per Claim 22, Chamberlain teaches:

"reading (E.g. see page 1, line 8) each relaxation (E.g. see page 10, lines 33-41, option – relax and see page 49, lines 11-13, relaxing address mode) instruction in the ordered sequence defined by the sequence of instruction counts;"

"where said relaxation instruction defines a relocation operation (E.g. see page 53, line 21), executing said relocation operation on section data (E.g. see page 16 line 29 to page 17, line 2) defined in one or more previously read relaxation instructions (E.g. see page 40, lines 1-12);"

"where said relaxation instruction defines section data (E.g. see page 16 line 29 to page 17, line 2) , copying said section data to said executable program, said section data being relocatable by subsequent previous relocation operations (E.g. see page 33, lines 34-35)."

5. Claims 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chamberlain in view of Charles et al., US Patent No. 6,314,564 (hereinafter Charles).

As Per Claim 8, the rejection of claim 1 is incorporated and further Chamberlain does not explicitly disclose accessing a stack. However Charles, in analogous art, teaches "accessing a

stack." (E.g. see Abstract and associated text). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Charles into the system of Chamberlain, by accessing a stack. The modification would have been obvious because one of ordinary skill in the art would have been motivated so that by adding stack operations to the relocation entries, postfix notation (also known as "reverse Polish notation") can be utilized to allow the resolution of the arbitrarily-complex expressions during the linking operation and within the object file itself (E.g. see Abstract and associated text).

As Per Claim 9, the rejection of claim 8 is incorporated and further Charles teaches: "said condition is determined according to a value of a top of said stack." (Again see Claim 8 as noted above and FIG.2, line 6 and associated text).

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kuo-Liang J Tang whose telephone number is (571) 272-3705. The examiner can normally be reached on 8:30AM - 7:00PM (Monday – Thursday).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Dam can be reached on (571) 272-3695. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kuo-Liang J. Tang

Software Engineer Patent Examiner

WEI Y. ZHEN
PRIMARY EXAMINER